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Massively Parallel Spatial Light Modulation-based Optical Signal Processing

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A new optical parallel arithmetic processing scheme using a nonholographic optoelectronic content-addressable memory (CAM) was proposed. The design of a four-bit CAM-based optical carry look-ahead adder was studied. Compared with existing optoelectronic binary addition approaches, this nonholographic CAM scheme offers a number of practical advantages, such as faster processing speed and ease of optical implementation and alignment. For an adddition of numbers longer than four bits, by incorporating the previous stage's carry, a number of four-bit CLA's can be cascaded. Experimental results were also demonstrated. One paper to the Optics Letters was published.

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Because of the lack of fast, accurate and large dynamic range analog-to-digital devices, optical implementation of the digital multiplication through analog convolution (DMAC) algorithm yields a slow digital multiplier. By replacing both the optical adder and A/D converter arrays by an optical combinatorial logic counter array, a new optical fast digital multiplication method was studied. Compared to the existing optical DMAC scheme, the new method promises both higher processing speed and accuracy. A comparison of this and some of the other optical and electronic fast digital multiplication schemes was also detailed. One paper to the Applied Optics was published.

Two new optical free-space collinear cross-over interconnect schemes were suggested. The first optical implementation uses mirrors and beam-splitters, while the second uses a Fresnel zone plate and lens combination. Both schemes allows for practical cascading to form multistage interconnect networks. The Fresnel zone plate based approach has an additional advantage, e.g. it can perform a 2D cross-over of 1D folded data so that the overall interconnect throughput is greatly increased. Design issues of such interconnects are addressed and proof-of-principle experiments were demonstrated. One paper to the Applied Optics is to be published in Apr. 1991.

Based on a electronically addressed spatial light modulator as an input device, a degenerate photorefractive optical phase conjugator, a new real-time coherent optical Wigner distribution and ambiguity function generation method for both 1D and 2D complex signals was proposed. As compared to all the existing Wigner methods, the new scheme allows for processing real-time phase-only as well as general complex signals. The new method can also be extended to perform ambiguity function evaluation of complex signals. Experimental results of the processor were presented. One paper to the Applied Optics was published.

A novel optical analog-to-digital (A/D) conversion scheme that uses a real-time theta modulation followed by a table look-up was investigated. As a fast theta modulator, a wide-band acousto-optic (A-O) deflector that performs a voltage to optical beam

deflection angle mapping, was used. Using a GaP A-O deflector, a proof-of-principle 6-bit A/D converter was experimentally demonstrated. Design issues and device fundamental limits were studied. One paper summarizing the study was published in Applied Optics.

The existing linear and rectangular processor distribution topologies for optical interconnects, although promising in many respects, can not solve problems such as clock skews, the lack of supporting elements for efficient optical implementation, etc. The use of a ring array processor distribution topology, however, can overcome these problems. One effort of studying the ring array topology was conducted with an aim of implementing various fast clock rate, high performance, compact optical networks for digital electronic multiprocessor computers. Practical design issues are addressed. A 36 node LED and Si PIN diode based ring interconnect network was experimentally fabricated and tested. A detailed research report was published in Applied Optics.

Based on our preliminary study of the ring array processor distribution topology, a compact reflective ring array interconnect was designed. The designed network can be reconfigured to perform the task of either a nearest neighbor interconnect or a plus-minus 2I interconnect. Our system study has shown that the design of the supporting optical imaging system for the proposed architecture is easier to be handled that that using a conventional rectangular array topology. Design principles for both the individual optical components and the entire optical system was carried out using the ZEMAX software. The network performance parameters, such as the diffraction- and aberration-related processing capabilities, the optical transmitter coupling efficiency, the optical free-space power distribution loss, the detector dynamic range requirement, and the power-dependent elemental-bit-rate, are analyzed. The report summarizing the study has been submitted to and accepted by the Applied Optics for publication.

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Recently, we have also investigated the possibility of implementing an optical shared content addressable memory (S-CAM) processor based on simple and efficient optical switches and free-space optical components. Electronic version of a CAM is usually based on the use of a digital programmable logic array (PLA) which only allows sharing among parallel I/O's in the time domain. Many computation applications, however, do require parallel sharing of memory information among various processors. Free-space optics provides such inherent parallelism to implement the sharing. In this study, we took a specific application example of building an N-bit modified signed digit adder using the S-CAM method. We showed that using an electronics scheme without suffering a speed loss, N PLA's each of 1K AND-OR switches must be employed. When the same calculation was performed using an optical S-CAM, a single 1K AND-OR switch array together with an appropriate space multiplexing scheme is sufficient. We then studied optical architectures to implement such a S-CAM and suggested and analyzed an optical matrix-product-based processor. The conclusion of the analysis is that the power consumption and the diffraction related cross-talk are the two dominant factors limiting the capacity of the optical S-CAM. It is possible to implement an optical S-CAM with a capacity to process 64 simultaneous memory access operations each of 32-bit in length with a 10^{-15} cross-talk error rate and in a 50 MHz read-out rate. A smaller scaled S-CAM was experimentally constructed to perform addition and subtraction of 8-bit MSD numbers in parallel. The detailed information was summarized in a paper submitted to the Applied Optics.

Publications: (only those which have not been reported to AFOSR)

* "Free-space optical collinear crossover interconnects" Y. Li and B. Ha, Applied Optics, 30 (1991) pp.3288-3293.

* "Ring-array processor distribution topology for optical interconnects," Y. Li, B. Ha, T. Wang, S. Wang, A. Katz, X. J. Lu, and E. Kanterakis, Applied Optics, 31 (1992) pp. 5548-5558.

* "Reflective optical ring array interconnects: an optical system design study," B. Ha and Y. Li, Applied Optics, 32 (1993) in print.

* "Parallel MSD arithmetic using an opto-electronic shared content-addressable memory procesor," Y. Li and B. Ha, submitted to Applied Optics for publication.